Fabrication of 200 to 2700 GHz Multiplier Devices using GaAs and Metal Membranes

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***Abstract* — Multiplier device fabrication techniques have been developed to enable robust implementation of monolithic circuits well into the THz frequency range. To minimize the dielectric loading of the wave guides, some circuits are realized entirely on a 3μm thick GaAs membrane with metal beamleads acting as RF probes and DC contact points. Other designs retain some thicker GaAs as a support and handling structure, allowing a membrane of bare metal or thin GaAs to be suspended across an input or output wave guide. Extensive use is made of selective etches, both reactive ion (RIE) and wet chemical, to maintain critical dimensions. Electron beam (e-beam) lithography provides the small contact areas required at the highest frequencies. Planar multiplier circuits for 200 GHz to 2700 GHz have been demonstrated using a variety of metal and GaAs membrane configurations made available by these fabrication techniques.**

I. Introduction

Millimeter and submillimeter heterodyne observations will improve our understanding of physical phenomena present in the universe, the solar system and Earth's atmosphere. To aid these studies, several space missions will soon fly instruments with heterodyne receivers working at frequencies up to 2.5 THz (FIRST, EOS-MLS, ROSETTA). High frequency non-cryogenic mixers and local oscillators (LO) are critical to the successful implementation of these missions. The goal of the technology development presented here is to enable design, fabrication, and robust implementation of solid-state components into the terahertz range.

For years, Schottky mixers developed for terahertz applications have employed point-contact single diodes. Similarly, development of high frequency multiplier sources also has relied on whisker contacted Schottky diodes. Though these whisker-based multiplier circuits have worked at frequencies as high as 1395 GHz (about 17 μW of power with an input power of 7 mW [1]), assembly tolerances are extremely tight and can substantially affect RF performance. Moreover, multiple diode configurations are difficult to implement, and reliability and bandwidth limitations continue to be a concern. To overcome these drawbacks, the monolithic membrane-diode (MOMED) process was developed, integrating Schottky diode mixers with RF filter circuitry on a 3-micron thick GaAs membrane suspended across a frame [2]. Mixer circuits based on this technology have shown excellent performance at terahertz frequencies [3]. In extending the MOMED technology to making multiplier circuits, we have increased design flexibility by introducing metal membrane structures and reconfiguring or, for some circuits, eliminating the thick GaAs support frames. Fabrication details for circuits from 200 GHz to 2.7 THz will be discussed.

II. Fabrication Technology

Our standard fabrication process for multiplier diode makes use of optical lithography and conventional epitaxial layer designs. To accommodate some of the demands of terahertz circuit designs, electron beam lithography is inserted into the process along with more complex epitaxial layers to allow for GaAs membrane definition. For convenience, the former process is designated the Low Frequency Process and the latter the High Frequency Process. Figs. 1 and 2 illustrate the process steps detailed below.

A. Low frequency process

At the lower frequencies (200-800 GHz), having the diode on extremely thin GaAs is not necessary and, for thermal reasons, may not be desirable. GaAs membranes, therefore, have not been incorporated into these designs, while metal membranes for the passive circuitry have been.

The starting material is semi-insulating GaAs with epitaxial layers grown by MBE or MOCVD. The diode structure consists of (1) a ~ 200nm thick n-type Schottky layer doped 2-5 $x10^{17}$ /cm^3 on top of (2) a heavily doped ($5x10^{18}$ /cm^3) ~1.5 micron thick n+ contact layer grown on (3) a 50nm $Al_{0.5}Ga_{0.5}As$ etch-stop layer. The ohmic contacts are an alloyed Au/Ge/Ni/Ag/Au metalization,

recessed into the n+ GaAs layer. Device mesas are defined using a selective dry etch of BCl_3, SF_6, and Ar in an electron cyclotron resonance (ECR) reactive ion-etch system (RIE). This etch slows sufficiently when the AlGaAs layer is reached so that mesa heights are quite uniform across the wafer. An airbridge process is used to define the anodes and the interconnect metal in the same process step. A first layer of photoresist is patterned then reflowed to form the sacrificial support for the airbridges. A second layer of patterned photoresist provides the stencil for the Ti/Pt/Au Schottky and interconnect metal.

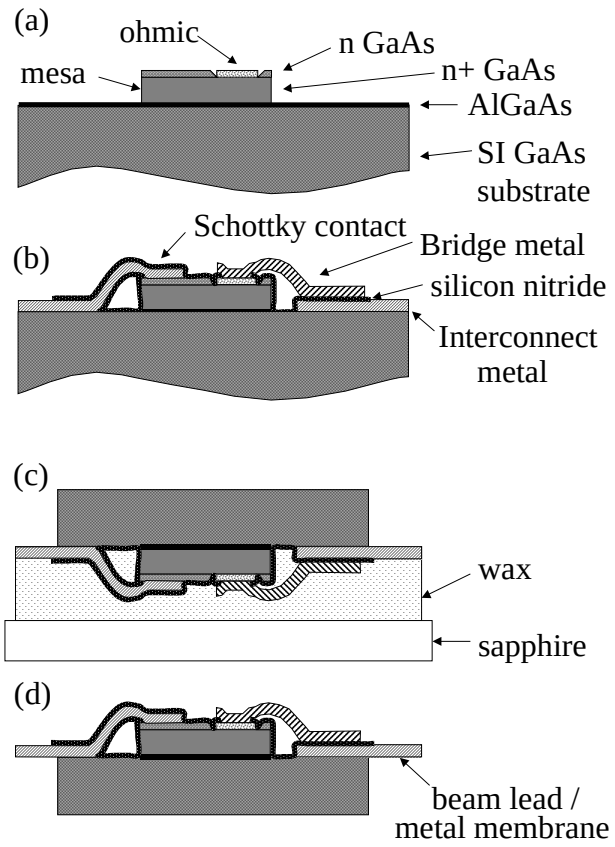


Fig. 1 Low Frequency process. (a) Ohmic and mesa definition. (b) Interconnect metal and air-bridged Schottky deposition, followed by passivation and bridge metal definition. (c) Backside thinning and device separation. (d) Release of device from carrier wafer.

Following Schottky metalization and lift-off, silicon nitride is deposited using plasma enhanced chemical vapor deposition (PECVD). This acts as the dielectric for any required MIM capacitors in addition to passivating the diodes. A subsequent air-bridged metal step forms the top contact to the capacitors in addition to providing connections to the on-mesa ohmic metal areas.

The wafer is next mounted topside-down, using wax, onto a carrier wafer, e.g. silicon, glass or sapphire. The GaAs substrate is thinned to the desired thickness (12-50 μm) by lapping, polishing and wet etching. The sample is then patterned and etched by RIE where the GaAs from between the circuits and beneath some of the interconnect metal is removed, to form the metal membranes and beamleads. At this point the circuits are separated and can be removed from the carrier wafer by dissolving the mounting wax and collecting the chips on filter paper. RF measurements of circuits based on some of these chips have been reported earlier [4] –[5].

B. High Frequency process

Wafers used in the fabrication of GaAs membrane-based circuits have additional epitaxial layers consisting of a 3μm thick undoped GaAs membrane layer supporting the diode layers and a 400nm thick lower AlGaAs etch-stop layer. The ohmic contacts and mesas are defined in the same manner as for the Low Frequency process, however the interconnect and anode metals are deposited in two separate steps. The interconnect metal is deposited to a thickness equal to the height of the mesas. This is important for the anode definition, where the sample is covered with over 3 μm of PMMA, which is subsequently thinned using acetone spray, until the tops of the mesas and interconnect metal are just exposed. This lower layer of PMMA forms a support for the PMMA/copolymer/ PMMA tri-layer that is used for the electron-beam defined anodes. This resist structure allows the Ti/Pt/Au anode metal to bridge the gap between the interconnect metal and the actual Schottky contact area on the active mesa. Fig. 3 shows the anode bridge of a 2.4 THz doubler circuit. At this frequency Schottky contact dimensions are a few tenths of a micron, necessitating the use of e-beam lithography in their definition. The circuit is then passivated and capacitors are defined as in the Low Frequency process.

The first membrane-related processing step lithographically defines the membrane areas of the circuits from the topside of the wafer. An RIE of CF_4/O_2 is used to remove the silicon nitride layer, followed by an ECR RIE of the 3μm GaAs membrane layer, again using $BCl_3/SF_6/Ar$, in order to stop on the lower AlGaAs etch stop layer. By defining the membrane during front-side processing of the sample rather than with backside lithography, critical spacing between the circuit elements and the membrane edge can be maintained. However, the wafer topography following the membrane etch requires that the final front-side metalization, to define additional circuit beam leads, be air-bridged from the top of the vertical-walled membrane layer to the field area, 3μm

below. This 1μm thick metal layer provides bias connections, mechanical support, RF tuning elements and feed antennas for the circuits.

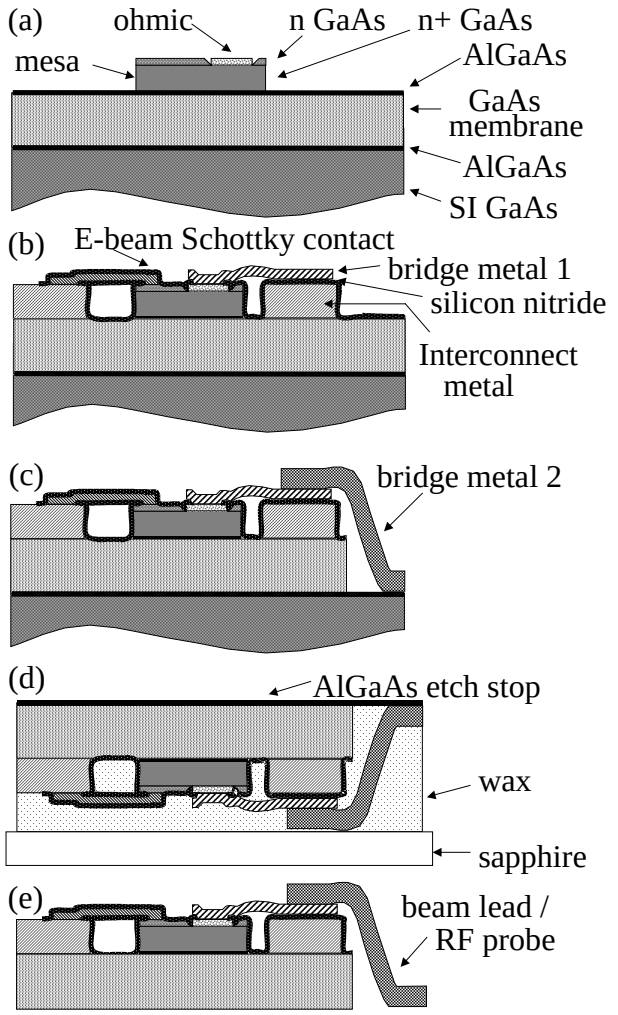


Fig. 2 High Frequency process. (a) Ohmic and mesa definition. (b) Interconnect metal and e-beam-defined Schottky deposition, followed by passivation and bridge metal 1 definition. (c) Membrane layer etch and bridge metal 2 deposition. (d) Removal of substrate with selective etch. (e) Release of device from carrier wafer.

As with the Low Frequency process, the wafers are wax-mounted to a carrier wafer and thinned. The wafers are then patterned and a selective wet etch of H_2O_2 and NH_4OH is used to remove GaAs from between the devices and beneath certain GaAs membrane regions. The lower AlGaAs layer protects the 3 μm membrane by acting as an etch stop. A brief non-selective etch (phosphoric acid/hydrogen peroxide/water) is then used to remove the AlGaAs etch stop. If necessary, the GaAs membrane layer can be removed from certain interconnect metal regions to create additional beamleads.

Again, the mounting wax is dissolved and the chips collected on filter paper.

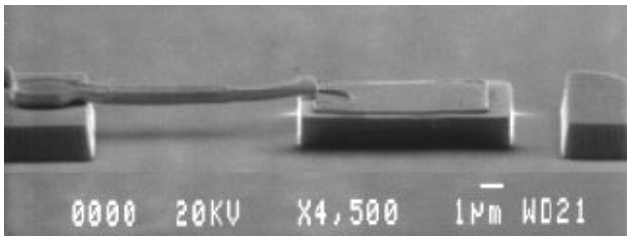


Fig. 3. SEM image of one diode in a 2.4THz doubler circuit. At the center is the diode mesa mostly covered by the ohmic contact metalization. The anode finger bridges from the interconnect metal, at left, to the 0.14 μm by 0.6 μm Schottky contact on the GaAs mesa.

III. Circuits

A. 200 and 400 GHz doublers

Fig. 4 shows a picture of a completed 400 GHz doubler chip mounted in a wave guide block. The diodes for this circuit are fabricated on one end of a 50μm thick support frame. The metal membrane for the low-pass filter and out-put probe is suspended across the GaAs frame. Beamleads provide ground and DC bias contact. Additional beamleads help to support the chip in the block, making assembly very simple. A similar configuration has been used to make a 200 GHz doubler and to design some 800 GHz circuits currently in fabrication.

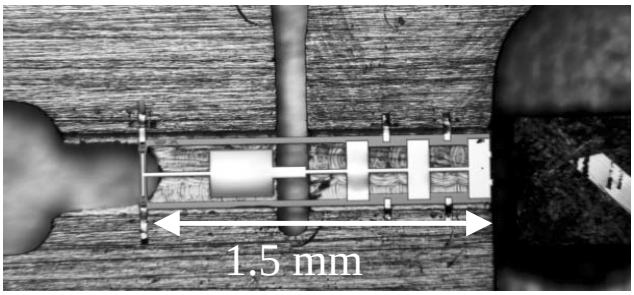


Fig. 4 Mounted 400 GHz doubler chip. Diodes are fabricated on the end of the frame to the left. The output probe (center) is visible spanning the output waveguide. At 380 GHz an efficiency of 20% with 8mW output was measured when cooled to 120K.

B. 1200 GHz tripler

Fig. 5 shows a picture of a completed 1200 GHz tripler device before mounting in a split-wave guide block. The diodes and matching circuit are on a 3 μm thick GaAs membrane that will be suspended across a channel in the block. The small size of the chip allows for the complete elimination of any thick GaAs support structure. Two large beam leads provide the mechanical support and ground contacts to the block, while two narrow beamleads act as RF probes in the input and output waveguides. A similar configuration has been used in the design of a 2400 GHz doubler chip. Waveguide blocks are currently in fabrication for this circuit.

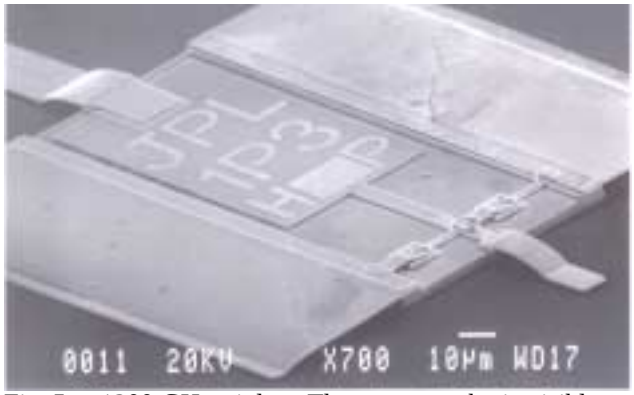
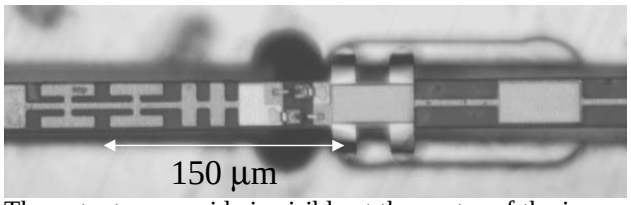


Fig. 5 1200 GHz tripler. The output probe is visible on the right. Output powers of >60μW have been measured.

Fig. 6 GaAs membrane section of a 2700 GHz tripler.



The output waveguide is visible at the center of the image, behind the diode pair, with backshort beamleads just to the right.

C. 2700 GHz tripler

Fig. 6 shows a detail of a completed 2700 GHz tripler chip mounted in a wave guide block. The diodes, band-pass filter, input probe and bias filter are contained on a 30 μm wide 800 μm long 3 μm thick GaAs membrane suspended across a 50 μm thick GaAs frame. Short beamleads protruding from the membrane near the diodes are grounded to the block to act as a back short. The diodes are suspended above the rectangular output waveguide, while a probe at the end of the bandpass filter spans the input waveguide. The circuit design and performance are detailed in [6].

IV. CONCLUSION

GaAs diode fabrication techniques have been developed that allow for robust multiplier circuit implementations into the terahertz regime. A variety of device architectures have been investigated to make the diode chips less of a driver in the final choice of circuit design. These monolithic multiplier chips make use of GaAs and metal membranes to decrease the dielectric loading of the circuits. Beamleads are used extensively to provide simple contacting schemes and support structures for the chips. Using these techniques, we have demonstrated planar multiplier circuits for 200 GHz to 2700 GHz.

ACKNOWLEDGEMENT

We would like to acknowledge Neal Erickson (UMass) and Peter Zimmermann (RPG) for contributing circuit designs. We also wish to acknowledge the technical help provided by Ray Tsang of JPL for circuit assembly, David Pukala for RF testing, and P. Bruneau for multiplier block fabrication. The research described in this publication was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration

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